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METHOD OF MAKING FIELD EFFECT TRANSISTORS HAVING SELF-ALIGNED SOURCE AND DRAIN REGIONS USING INDEPENDENTLY CONTROLLED SPACER WIDTHS

Abstract

A method is provided for defining spacings between the gates of field effect transistors (FETs) of an integrated circuit and the source and drain regions thereof, the spacings differing in width between a first FET and a second FET. The method includes forming gate stacks of the integrated circuit over a substrate, and forming first spacers on sidewalls of the gate stacks. Second spacers are then formed over the first spacers. Thereafter, source and drain regions of the first FET are formed in alignment with the second spacers of a first gate stack of the gate stacks. The second spacers are then removed from the first spacers of the gate stacks. Thereafter, the first spacers of a second gate stack are anisotropically etched in a substantially vertical direction to remove horizontally extending portions of the first spacers, and

source and drain regions of the second FET are formed in alignment with portions of the first spacers of the first gate stack which remain after the etching.